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7-23-02 #3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 040301/0487

In re reissue patent application of

Nobuo FUDANUKI et al.

Serial No: Not Yet Assigned

Application for reissue of U.S. Patent No. 6,054,872, granted April 25, 2002

Filed: Herewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT WITH MIXED GATE ARRAY AND STANDARD CELL

PRELIMINARY AMENDMENT

Commissioner for Patents
Box REISSUE
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-captioned application as follows:

IN THE CLAIMS

Please add claims 22-65 to the reissue application.

(Reissue Claim 22) The integrated circuit of claim 1, wherein each gate array basic cell has the same pattern of gate electrodes and the same pattern of impurity regions.

(Reissue Claim 23) The integrated circuit of claim 1, wherein said standard cells include a third type cell having a width different from the widths of the first type cell and the second type cell.